

## Synchronous DRAM Controller

For Video Image Processing in 64/128M

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Questions and/or comments may be directed to

**PEC Technologies**

**Engineering R&D Team**

**Email:** [info@pectechnology.com](mailto:info@pectechnology.com)

### Revision History

Rev.	Date	Author	Description
0.1	Feb.23 / 2009	PEC R&D Team	First Draft Release
0.2	Apr. 30 / 2009	PEC R& D Team	RTL modified for all parameters
0.3			Frame Controller Implemented With FIFOs

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## Introduction

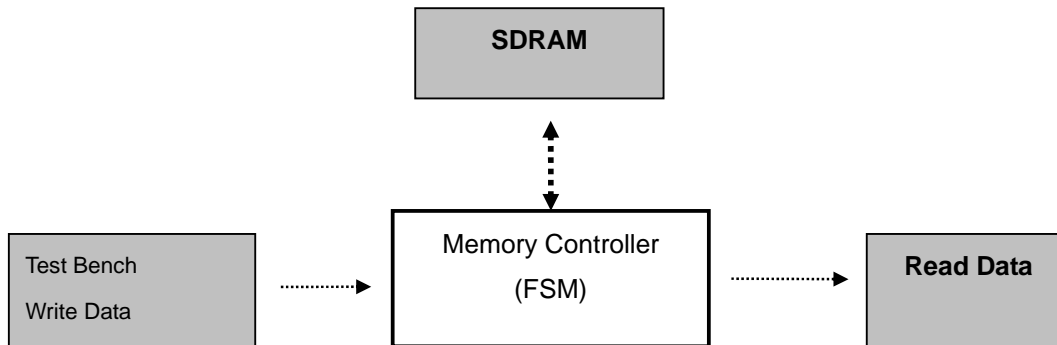
### FEATURES

- Performs pipeline sequencing in the Memory Controller.
- Generates SDRAM control signals and SDRAM command sequencing.
- Supports variable burst length, up to the maximum programmed in the LMR.
- Performs access direct forward work for image write/read in HDTV(1080p), UXGA(2048x1024) Video / Graphic Resolution.
- Timing that meets the requirements of the Samsung / Micron/ Hynix 64M / 128M SDRAM (LMR command parameters are embedded within the Address-Path module.)
- Optimized Video image Processing
- 4 Bank x 32bit x 2048 rows x 256(512M) columns, 64M / 128M.
- Supports all SDRAM Timing Parameters in configuration / Registers.

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### 2.1 Memory Controller –Top level



### 2.2 Parameter Configuration

Parameter	Description	Time
tRC	RAS Cycle time	>= 70ns
tRRD	RAS to RAS Bank activate delay	>= 20ns
tRCD	Activate to command delay - RAS to CAS delay	>= 20ns
tRAS	RAS Active time	>= 50ns
tRP	RAS Pre-charge time	>= 20ns
tMRD		>= 3 tCK(Clock Cycles)

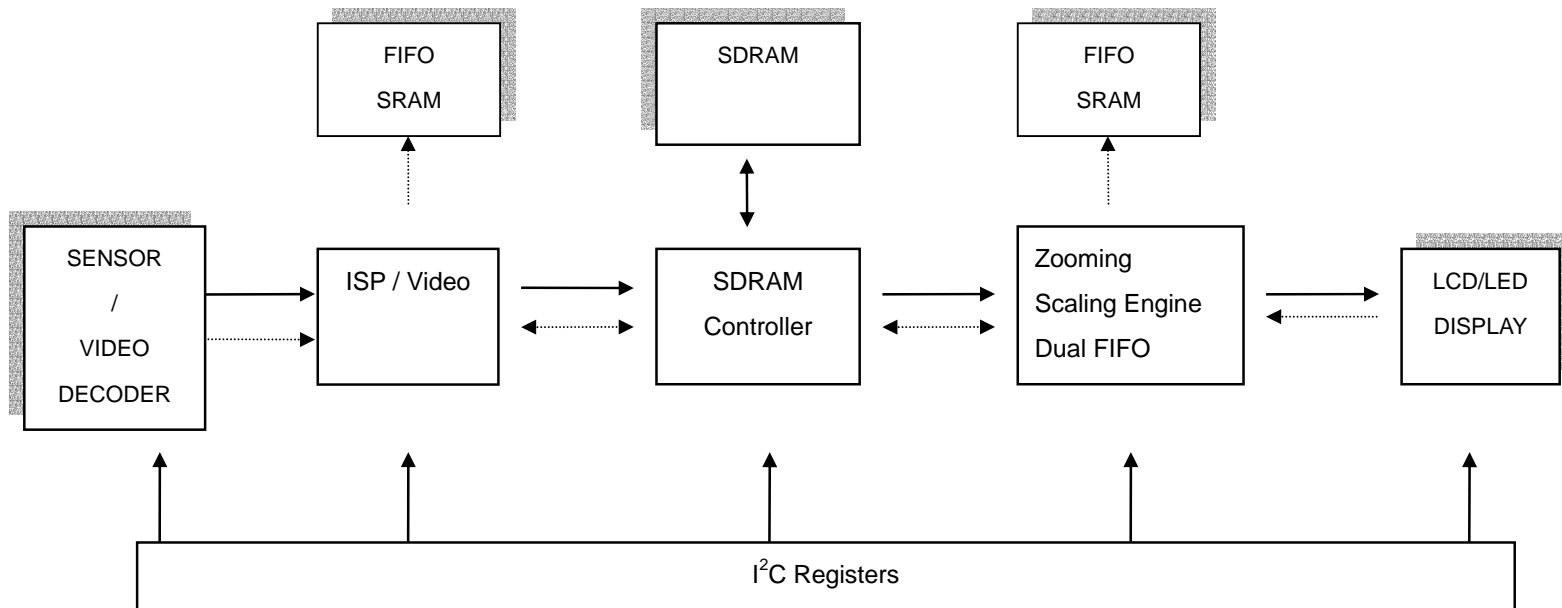
tREF	Refresh period for 4096 rows, so $64\text{ms}/4096 = 15.625\text{us}$ per row	$\leq 64\text{ms}$
tRFC	Row refresh cycle time	$\leq 80\text{ns}$
tSTARTUP_NOP	200000 ns	200 us
CLOCK_PERIOD	Operation Clock	7n ~ 15ns
CASWIDTH	width of CAS mode for MRS	1/2/3 tCK Clock Cycles

### 2.3 I/O Ports

1. Write \_ Request: Write Data Request, Write\_ Acknowledge
2. Read \_ Request: Read Data Request, Read\_ Acknowledge
3. SDRAM I/Os: CKE,  
CLK,  
CS\_n,  
BA[1:0],  
ADDRESS[10:0],  
RAS\_n,  
CAS\_n,  
DQ[31:0],  
DQM[3:0]

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**Application Architecture – Frame Controller Block Diagram.**



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### **Operations**

1. Supports 16M ~ 128M SDRAM (133Mhz) of Samsung, Micron, Hynix Vendors
2. Configurable for all parameters, Bank, Timing Parameters, Burst, CAS Latency.. etc.
3. Comfortable for all video image data

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## Usage Guide

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|----------------------------|-----------------------|
| 1. RTL Implementation      | VerilogHDL            |
| 2. Test bench (VerilogHDL) | ModelSim Verification |
| 3. Proto-Typing in FPGA    | Xilinx FPGAs          |